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What is claimed is:

1. A method of forming an interconnection line in a semiconductor device comprising:

forming a first etching stopper on a lower conductive layer which is formed on a semiconductor substrate;

forming a first interlayer insulating layer on the first etching stopper;
forming a second etching stopper on the first interlayer insulating layer;
forming a second interlayer insulating layer on the second etching stopper;
etching the second interlayer insulating layer, the second etching stopper, and
the first interlayer insulating layer sequentially using the first etching stopper as an
etching stopping point to form a via hole aligned with the lower conductive layer;

forming a protective layer to protect a portion of the first etching stopper exposed at the bottom of the via hole;

etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole;

removing the protective layer;

removing the portion of the first etching stopper positioned at the bottom of the via hole; and

forming an upper conductive layer that fills the via hole and the trench and is electrically connected to the lower conductive layer.

- 2. The method of claim 1, wherein the lower conductive layer includes a copper layer.
- 3. The method of claim 1, wherein the first etching stopper is formed of at least one of silicon nitride and silicon carbide

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- 4. The method of claim 1, wherein the first interlayer insulating layer is formed of a material having a low dielectric constant.
- 5. The method of claim 4, wherein the material having a low dielectric constant is carbon-doped silicon oxide (SiOC).
- 6. The method of claim 1, wherein the second etching stopper is formed of at least one of silicon nitride and silicon carbide.
- 7. The method of claim 1, wherein the second interlayer insulating layer is formed of a material having a low dielectric constant.
- 8. The method of claim 7, wherein the material having a low dielectric constant is carbon-doped silicon oxide (SiOC).
- 9. The method of claim 1, wherein the protective layer includes nonorgarnic spin-on dielectric (SOD).
- 10. The method of claim 9, wherein the nonorganic SOD is Hydrogen silsesQuioxane (HSQ).
- 11. The method of claim 1, wherein the step of forming the protective layer comprises:

forming the protective layer on the second interlayer insulating layer to fill the via hole; and

etching back the protective layer so that the upper surface of the protective layer is lower than the upper surface of the second interlayer insulating layer.

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- 12. The method of claim 11, wherein the etch back is performed by a wet etching method using a resist developer.
- 13. The method of claim 12, wherein the resist developer includes a tetramethyl ammonium hydroxide aqueous solution.
- 14. The method of claim 11, wherein the etch back is performed by a wet etching method using a HF solution diluted with water.
- 15. The method of claim 1, wherein the protective layer is removed by a wet etching method using a resist developer.
- 16. The method of claim 15, wherein the resist developer includes tetramethyl ammonium hydroxide aqueous solution.
- 17. The method of claim 1, wherein the protective layer is removed by a wet etching method using a HF solution diluted with water.
- 18. The method of claim 1, wherein the upper conductive layer includes a copper layer.